



2022 Update

# Product Technology Guide

The New Generation of  
Thin Film Electronics

***Fast. Flexible. Simple.***

Amorphyx   
*Simple. For a Change.*



October 2022

To Our Customers and Partners:

Amorphyx is an innovator at the intersection of materials science and electronics. The Company was founded in 2012 to leverage the benefits of amorphous metals in defining the new generation of thin film electronic device and circuit performance, cost and manufacturability.

The fundamental material properties of thin film semiconductors do not support the future of flexible integrated circuits - **Fast. Flexible. Simple.** While academia and the display industry focused on increasing thin film transistor performance through increasingly complicated metal oxide semiconductor materials, **Amorphyx chose the path of revisiting device physics.** Ten years later we have commercialized a family of technologies defining the path to future of thin film electronics in displays and the Internet of Things.

- a rethinking of metal oxide-based Thin Film Transistors **using standard thin film deposition techniques and equipment to incorporate new understandings of the use of high gate electric field strength for maximizing metal oxide TFT performance.**
- The Amorphous Metal IGZO TFT replaces LTPS TFTs in premium AMOLED and microLED displays. **With field effect mobility > 70 cm<sup>2</sup>/V-s at industry-standard stress performance,** IGZO AMeTFT enables 0.1-240Hz variable image refresh rate at reduced operating voltage from a process with no significant changes to existing TFT fabrication lines.
- Research and development of the **first commercially-viable quantum tunneling thin film electronic devices, realizing the integration of speed, flexibility and manufacturing simplicity** using the same materials set - amorphous metals and high-k dielectric oxides - as used in the gate structure of IGZO AMeTFT. The Amorphous Metal Nonlinear Resistor (AMNR) and the Amorphous Metal Hot Electron Transistor (AMHET) Define a path to tera-hertz speed capable switching, high refresh, high color, high mobility, displays on flexible materials.

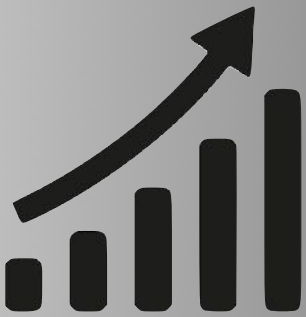
**AMNR, IGZO AMeTFT, IGZO AMeTFT 2T1C and “211” AMNR+AMeTFT data presented in this document is actual device data - not simulation results.** Amorphyx has collected extensive performance data over more than 400 development wafer lots - data that is available to customers for support of technology transfer and display development.

Amorphyx is leveraging AMNR and IGZO AMeTFT technologies into standard circuit cells for LCD, AMOLED and microLED applications - including utilizing the very fast switching speed of AMNR into pulse width modulation control of AMOLED and microLED pixels for further improvements in image quality and mobile device power consumption.

For more information on Amorphyx, please visit our website at [www.amorphyx.com](http://www.amorphyx.com). We are eager to create new relationships while expanding our current engagements as displays set the foundation for the new generation of consumer, commercial, industrial and medical electronics.

Kindest regards,

John Brewer  
CEO and President

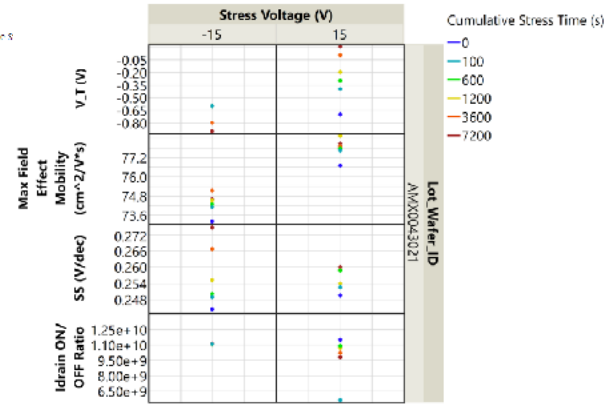
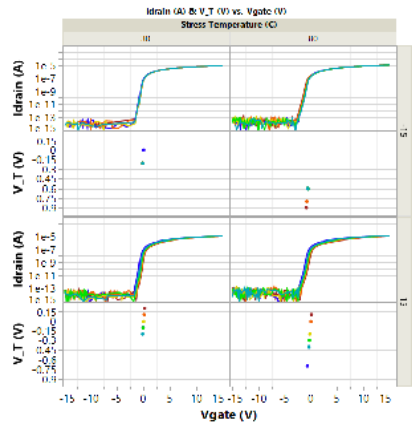


# Progress in 2022

IGZO-based TFT devices with  $\mu\text{FE} > 70$  and  $< 1\text{V}$   $V(\text{TH})$  bias stress shift operating in typical OLED/microLED pixel

$\mu\text{FE} > 70$  with  $20\text{V}/80^\circ\text{C}/7200\text{sec}$  PBTIS = 0.7V

$\mu\text{FE} > 40$  with  $30\text{V}/80^\circ\text{C}/7200\text{sec}$  PBTIS = 0.8V

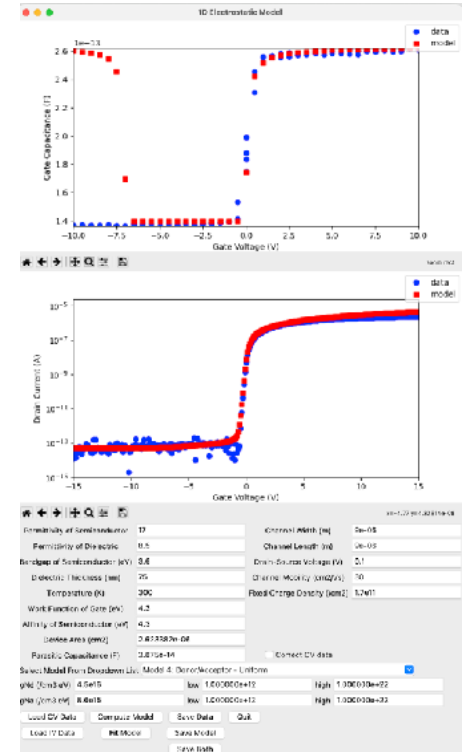


New theories in IGZO TFT device physics define mechanisms for IGZO AMeTFT performance

Read details in September 2022 issue of "Information Display": <https://sid.onlinelibrary.wiley.com/doi/10.1002/msid.1342>

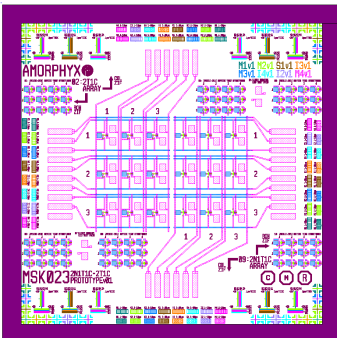


Analytics-based simulation linkage between film/processing parameters and device electrical performance

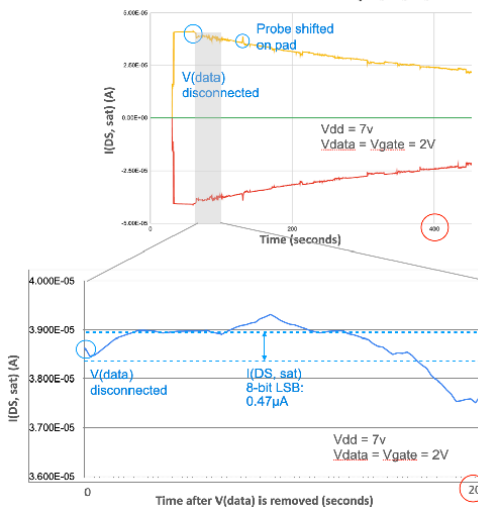


OLED/microLED proof-of-concept pixel circuits -

0.1-120Hz variable image refresh rate, scalable from smartphones to TVs



Development platform including 2T1C and 2T1 3x3 pixel arrays with microLED emitters. Available for customer evaluation under sampling agreement.



The use of amorphous gate metal and high-k dielectric oxide gate insulator combines the high electric field strength needed to maximize metal oxide performance with extremely low leakage current required for sub 0.1Hz image refresh rate.

IGZO AMeTFT device physics-based theoretical model links properties of thin films to device electrical performance parameters through Amorphyx's proprietary development database

# The Future is Smooth

The display industry's single greatest challenge for the last decade has been advancing semiconductor thin film transistor performance to meet consumer demand for higher quality images at reasonable price and power consumption points.

The industry's response has been to emphasize improvements to the semiconductor material. Amorphyx's response to this challenge is unique: **stop focusing on the semiconductor material for a solution. Instead, rethink the TFT itself.**

Amorphyx chose to focus on the TFT as a system instead of focusing on metal oxide materials. **The key learnings: the benefits of high gate electric field strength in generating exponential improvement in metal oxide TFT mobility.**

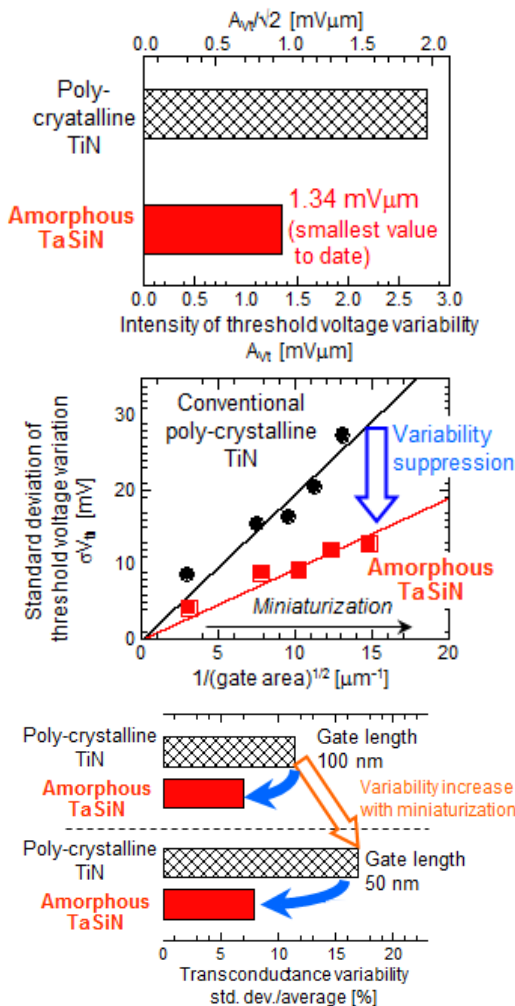
Amorphyx's technologies are built upon the benefits ultra-smooth amorphous metals create for thin film electronic devices.

- An order-of-magnitude increase over typical TFT operating electric field strength accesses **exponential increase in metal oxide TFT field effect mobility using standard thin film deposition techniques and equipment.** The same level of electric field strength makes the fastest, simplest thin film electronic devices possible - quantum tunneling switches and transistors.
- Thinner, high-k dielectric TFT amorphous gate insulators reduce mobility and threshold voltage variation limitations of silicon and metal oxide TFTs while meeting existing LTPS and IGZO TFT stress performance. The same combination of amorphous metals and high-k dielectric oxides support high-reliability quantum tunneling electronics.

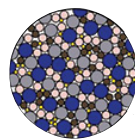
Amorphous metals are the foundation of the future of thin film electronic device performance - as they are for delivering Moore's Law benefits in VLSI FinFET CMOS technology. Through increasing the energy stored in the gate capacitance to achieve LTPS-grade field effect mobility while maintaining LTPS-grade operating bias stability, **amorphous metal-based devices define a new generation of thin film integrated circuits:**

**Fast. Flexible. Simple.**

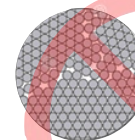
Amorphous metals create the bridge to the future of thin film electronics as quantum tunneling device speed and manufacturing simplicity drive an inflection point beyond semiconductors - enabling the future of flexible, high-performance displays and integrated circuits.



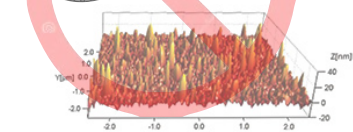
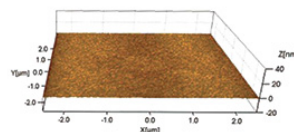
Research in VLSI CMOS FinFET structures validates the mobility and threshold voltage variability benefits of amorphous gate metals  
 (Source: "FinFET with the World's Smallest Characteristics Variability"  
[https://www.aist.go.jp/aist\\_e/list/latest\\_research/2013/20130326/20130326.html](https://www.aist.go.jp/aist_e/list/latest_research/2013/20130326/20130326.html))



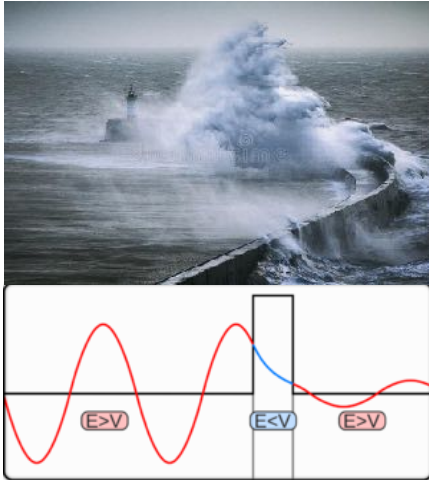
Amorphous Metal



Crystalline Metal

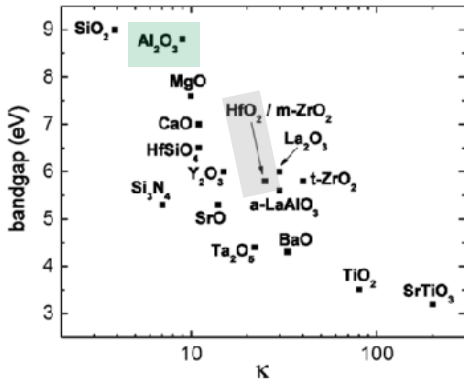


# Foundations



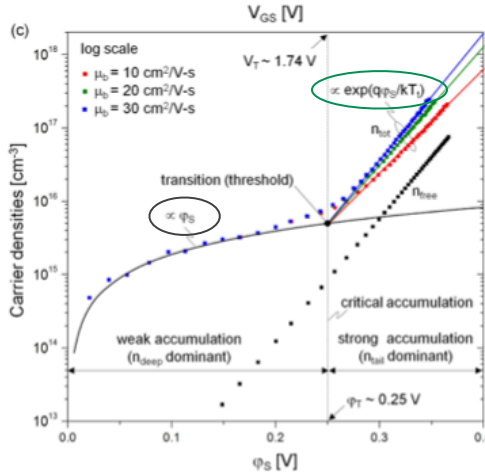
Quantum tunneling requires an electric field energy greater than the energy barrier presented by the insulator material.

This means **high electric field strengths** - making choice of insulator material, electrode metal smoothness critical



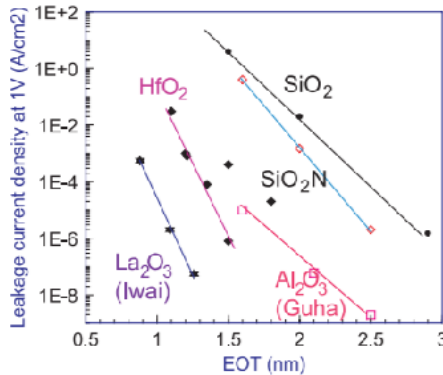
G. C. Jegert, "Modeling of Leakage Currents in High-k Dielectrics", thesis dissertation at Technical University of Munich, Dec. 2011.

The use of high electric field strengths requires insulators optimized for high breakdown voltage, in addition to high permittivity for minimizing device size and low leakage current. Amorphyx chose aluminum oxide for its family of thin film electronic devices - and chose titanium aluminide as the amorphous metal for its interfacial compatibility with aluminum oxide.



Lee and Nathan, "Conduction Threshold in Accumulation-Mode InGaZnO Thin Film Transistors", *Nature Scientific Reports*, 6-22567, Electrical Engineering Division, Department of Engineering, University of Cambridge, 2 March 2016.

IGZO AMeTFT utilizes the region of **exponential increase in carrier density with respect to surface potential** in delivering LTPS mobility with IGZO operating bias stress performance using high gate electric field strength.

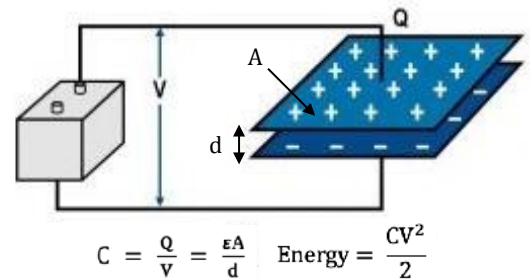


J. Robertson, "High dielectric constant oxides," *The European Physical Journal Applied Physics*, vol. 28, no. 3, pp. 265-291, Dec. 2004.

Amorphyx's groundbreaking family of thin film electronic devices are based on the same principles that have advanced "Moore's Law" in VLSI CMOS - **increasing transistor mobility through increasing gate electric field strength.**

Increasing electric field strength requires use of insulators capable of sustaining high energy levels and maximizing uniformity of electric field strength across the insulator area.

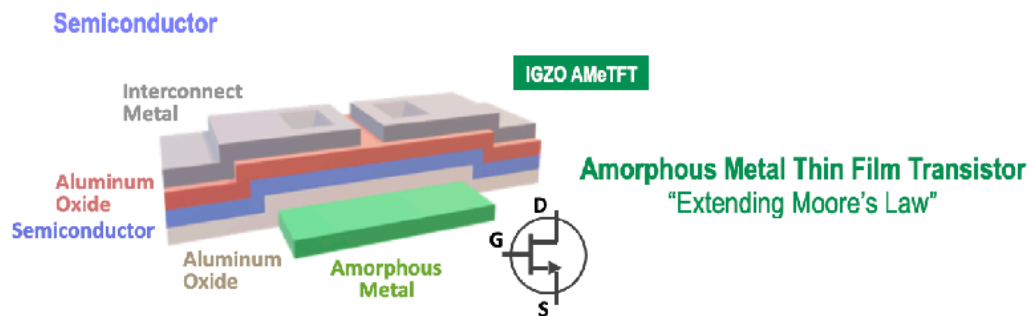
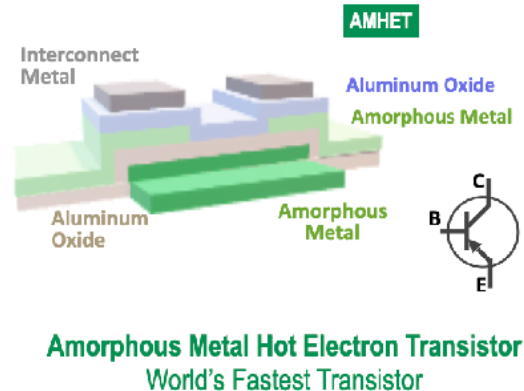
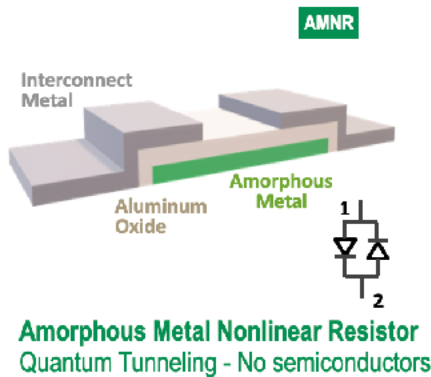
**Amorphous metal electrodes are critical in the fabrication of high electric field strength devices.** Their ultra-smooth surfaces ensure constant insulator thickness (d) across the entire area of the insulator. This ensures uniformity of stress across the insulator, maximizing insulator breakdown field strength and minimizing leakage currents.



Increasing insulator permittivity ( $\epsilon$ ) and reducing insulator thickness (d) through the use of amorphous metals **results in an order-of-magnitude increase in energy stored in the device.** This energy is transferred to the semiconductor using the gate electric field.

SiO <sub>2</sub>	$E_g$ (eV)	Band gap	9
	$\epsilon_{ox}$	Relative permittivity	3.9
Si <sub>3</sub> N <sub>4</sub>	$E_g$ (eV)	Band gap	5.3
	$\epsilon_{ox}$	Relative permittivity	7.5
Al <sub>2</sub> O <sub>3</sub>	$E_g$ (eV)	Band gap	8.8
	$\epsilon_{ox}$	Relative permittivity	9.3
HfO <sub>2</sub>	$E_g$ (eV)	Band gap	6
	$\epsilon_{ox}$	Relative permittivity	22.0

# The New Generation of Thin Film Electronic Devices



Amorphyx uses a single material stack - amorphous titanium aluminide metal and aluminum oxide - as the foundation for its family of high-performance high electric field strength thin film electronic devices.

Single-gate AMeTFT uses these materials to energize IGZO into its exponential region. Combining  $\text{Al}_2\text{O}_3$  high permittivity with a relatively thin 50-75nm gate insulator results in **an order-of-magnitude increase in gate electric field strength over the display industry's conventional single-gate IGZO TFT structures**. The amorphous metal gate's ultra-smooth surface enables thinner gate insulators without compromising the insulator's breakdown voltage performance.

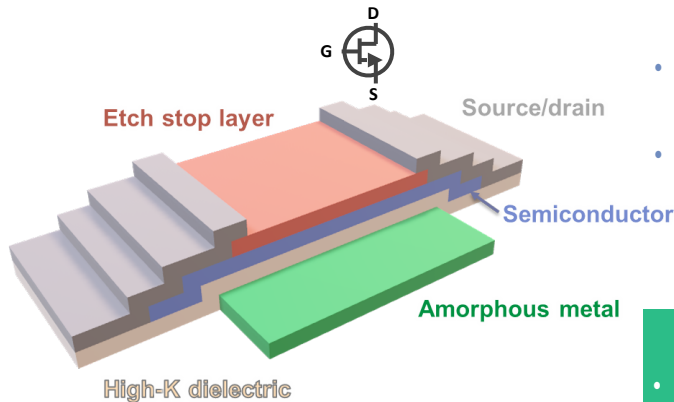
AMNR uses these materials to achieve "on" voltages suitable for mobile devices. Insulator thickness in the 10-20nm range ensures sufficient electric field strength to support Fowler-Nordheim field emission, while the amorphous metal's ultra-smooth surface **ensures uniform current density across the tunneling area** - critical for high reliability and stability performance.

AMHET is currently in its research phase. It integrates the proven AMNR device technology into a field emission-based Fowler-Nordheim tunneling transistor. AMHET's field emission mechanism ensures it to be the world's fastest transistor - in a simple structure and flexible materials stack. **Fast, flexible, simple - the ideal device for the future of integrated circuits.**

# Amorphous Metal TFT: LTPS Performance, a-Silicon Simplicity

**High-k dielectric**

- Al<sub>2</sub>O<sub>3</sub> 10-50nm
- Room Temperature Reactive Sputter



- Smooth interface increases effective semiconductor channel thickness, thus **increasing mobility**
- Ultra-smooth gate metal surface ensures ultra-smooth gate insulator-semiconductor interface - improving mobility and operating stress performance

**High-k dielectric**

- Al<sub>2</sub>O<sub>3</sub> 50-100nm
- Room Temperature Reactive Sputter

- **Reduces leakage current, V<sub>TH</sub> variations** related to silicon-based gate insulators
- Enables thinner gate insulator, **increasing mobility**

**Amorphous metal gate**

- TiAl<sub>3</sub> 50-75nm
- Room Temperature Sputter
- <5Å RMS surface roughness
- Wet or dry etch

## New Gate Materials Set Brings Moore's Law Improvements to Amorphous Silicon and Metal Oxide TFTs

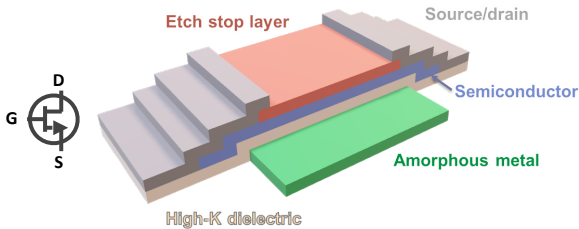
### Key Benefits

**Increases Image Resolution, Refresh Rate**

**Improves Manufacturability**

- Leverages benefits of amorphous metal gate, high-k dielectric gate insulator
  - Increased gate electric field energy increases conversion of available carrier density in IGZO to free electron density for I(DS)
- High-k dielectric gate insulator minimizes leakage current due to interactions with semiconductor
  - Supports 0.1-240Hz variable image refresh rate
- Amorphous metal gate
  - Ultra-smooth gate metal enables thinner gate insulator = increased mobility, reduced V<sub>TH</sub> variation across display
- Supports existing TFT bottom and top gate structures
- <50% of mask count for LTPS TFT - similar to current metal oxide stacks

# IGZO AMeTFT Performance: High Mobility with Excellent Stability

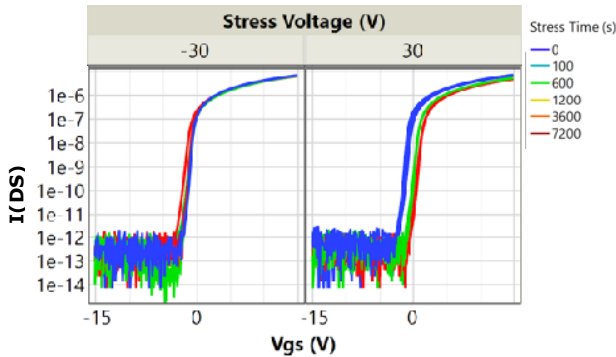
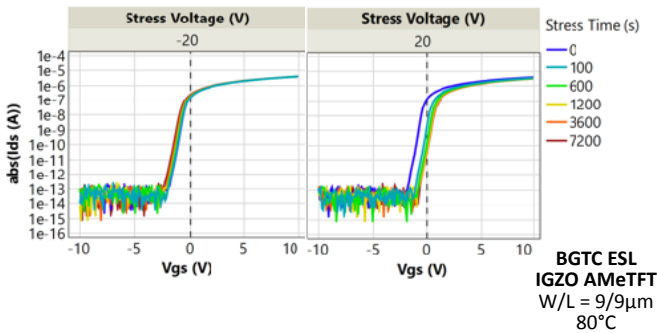


Amorphous Metal Gate's ultra-smooth surface enable thin Gate Insulator in standard TFT structures. The resulting increase in energy stored in the gate capacitance translates through the gate electric field to achieve bulk accumulation in metal oxide semiconductors at thicknesses >50nm.

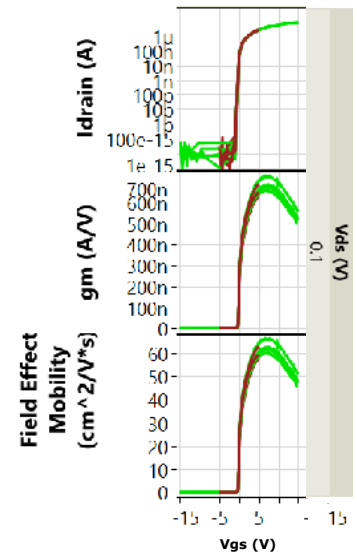
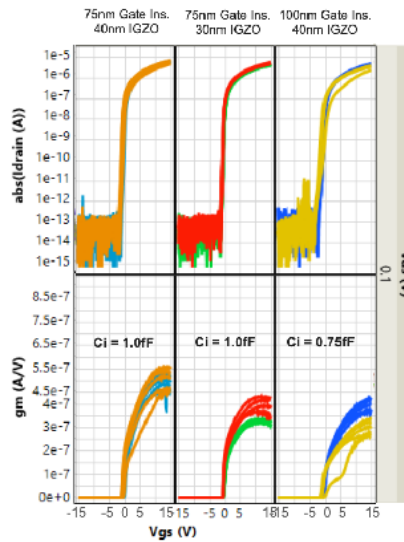
This increases  $I(DS, sat)$  for a given set of channel dimensions - doing so at lower  $V(GS)$  than traditional metal oxide TFTs - while dramatically increasing transconductance and mobility.

High-k dielectric oxide Gate Insulator results in higher breakdown voltage for thin Insulator, enabling gate electric field strengths an order of magnitude larger than traditional metal oxide TFTs while dramatically reducing leakage current.

Thin Gate Insulator leads to increased mobility, while balancing the oxygen content of gate insulator, metal oxide semiconductor and etch stop layer avoids compromising PBTIS, NBTIS, SS performance.



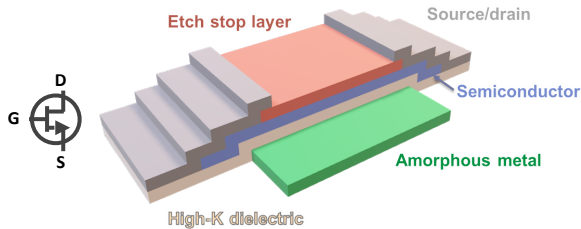
Increasing gate electric field strength transitions from a somewhat linear relationship with  $g_m$  to an exponential relationship as gate insulator thickness is reduced. Transconductance thus increases faster than gate capacitance, resulting in increased field effect mobility with thinner gate insulator - > 70  $cm^2/V\cdot s$  - with <1V 20V PBTIS.



The data also shows increasing  $g_m$  and  $I(DS, sat)$  with increasing IGZO thickness - indicating a bulk accumulation thickness > 40nm - promising further increase in  $\mu_{FE}$  with increasing IGZO thickness.



# IGZO AMeTFT Performance: High Mobility with Excellent Stability



TFT Technology Comparison

Performance Specification	Symbol		SHARP LTPS TFT (W/L = 10/7.5μm)	SHARP "IGZO 7" TFT (W/L = 10/7.5μm)	LG Display IGZO TFT (W/L = 26/10μm)	Samsung Display IGZO TFT (W/L = 2.6/4μm)	CEC Panda IGZO TFT (W/L = 10/6μm)	IGZO AMeTFT (W/L = 9.0/9.0μm)	Goal	Units
Threshold Voltage	V(TH)		1.5	1.0	0	0.75	0	0	0	Volts
Drain-Source Current	I(DS)									
		V(GS) = 1V V(DS) = 0.1V		0.1	0.1	0.5	0.01	0.5		μAmps
		V(GS) = 5V V(DS) = 3V						75	100	μAmps
		V(GS) = 20V V(DS) = 10V	450	450	20	50	20			μAmps
Field Effect Electron Mobility	μ(FE)	V(GS) ≥ V(TH)	90	40		8	13	75	100	cm <sup>2</sup> /V-s
On-Off Current Ratio	I(ON)/I(OFF)	V(ON) ≥ V(TH) V(OFF) = 0V	10 <sup>6</sup>	>10 <sup>9</sup>		>10 <sup>9</sup>		>10 <sup>9</sup>	>10 <sup>9</sup>	
Subthreshold Swing	SS		0.3	0.1				0.1	0.1	V/dec
Operating Stress	NBTS									
-10V Stress		-15 ≥ V(GS) ≥ +15V V(DS) = 0.1V						(7200 sec 80°C) -0.25	(7200 sec 80°C) -0.25	Volts
-20V Stress		-15 ≥ V(GS) ≥ +15V V(DS) = 0.1V				(3600 sec 60°C) -0.75		(7200 sec 80°C) -0.5	(7200 sec 80°C) -0.5	Volts
-30V Stress		-15 ≥ V(GS) ≥ +15V V(DS) = 0.1V	(3600 sec, 50°C) -0.4	(3600 sec, 60°C) -0.4	(3600 sec, 60°C) -0.1		(7200 sec, 60°C) -0.4	(7200 sec 80°C) -0.5	(7200 sec 80°C) -0.5	Volts
	PBTS									
10V Stress		-15 ≥ V(GS) ≥ +15V V(DS) = 0.1V						(7200 sec 80°C) 0.25	(7200 sec 80°C) 0.25	Volts
20V Stress		-15 ≥ V(GS) ≥ +15V V(DS) = 0.1V				(3600 sec 60°C) 0.5		(7200 sec 80°C) 0.5	(7200 sec 80°C) 0.5	Volts
30V Stress		-15 ≥ V(GS) ≥ +15V V(DS) = 0.1V	(3600 sec, 50°C) 0.8	(3600 sec, 60°C) 0.4			(7200 sec, 60°C) 0.4	(7200 sec 80°C) 1.7	(7200 sec 80°C) 0.5	Volts

Sharp LTPS, IGZO 7 TFT data from "Development of High Quality IGZO-TFT with Same On-Current as LTPS", 2020 Society for Information Display International Symposium Digest of Technical Papers, September 2020.

Samsung Display data from "High Mobility Oxide Thin-film Transistors for AMOLED Displays", 2022 Society for Information Display Technical Symposium, May 2022.

# Tunneling Electronics: Unequaled Speed with Simplicity

**Amorphous semiconductor mobility limits thin film transistor performance while driving increasing complexity in TFT manufacturing** - contradicting the path towards high-performance flexible integrated circuits. Our goal: define the future of flexible integrated circuits through the elimination of their largest impediment - the reliance upon semiconductor materials in thin film transistors.

The first commercially viable Fowler-Nordheim quantum tunneling devices

- overcome the mobility limitations of semiconductors,
- de-emphasize vertical alignment tolerances, and
- redefine switching speed

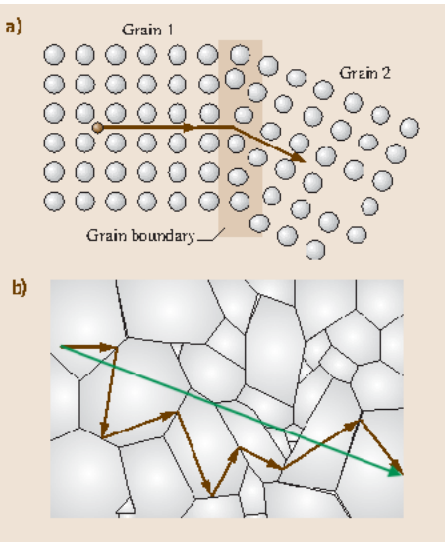
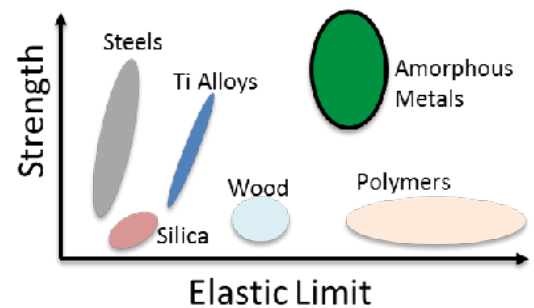
**maximizing variable image refresh rate performance** at both low and high rates to drive gaming-like image quality and **dramatic improvements in mobile device battery life**.

All in a fully amorphous material stack ideal for flexible substrates.

We demonstrated the industry's first quantum tunneling backplane at Display Week 2018 (AMNR-IPS LCD 85ppi 5" 60Hz) produced in collaboration with the world's largest display manufacturer - a testament to **the ability of Amorphyx and its technologies to leverage existing display manufacturing infrastructure**. The AMR-IPS LCD supports image refresh rates below 0.1Hz and as fast as the liquid crystal can support.

## FLEXIBLE

Amorphous metals uniquely combine two properties of materials: they are **stronger than steel while being as flexible as polymers**. This combination makes quantum tunneling electronic devices ideal for flexible displays.



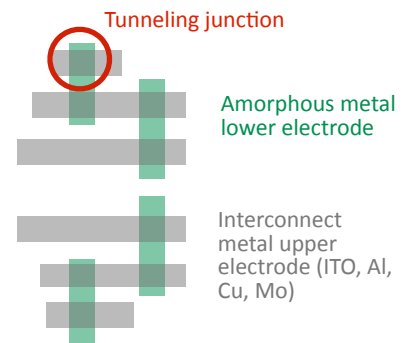
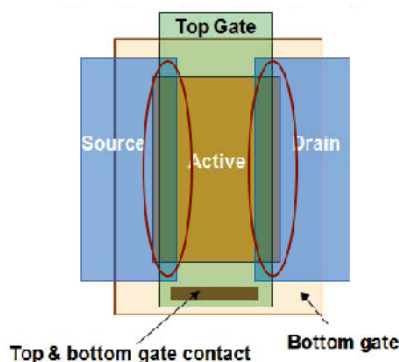
## FAST

Electrons conduct along grain boundaries in a semiconductor (**brown arrows**). **But tunneling electrons travel in a straight line through the material (green arrow)**. This is why tunneling electronic devices can switch at speeds far in excess of any semiconductor-based device.

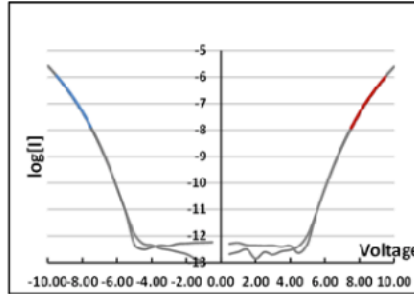
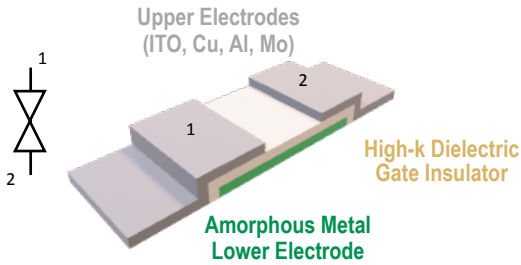
## SIMPLE

A pair of AMNRs replaces a TFT in a pixel circuit.

In a TFT (top-down view in first image), the critical vertical alignment dimension of gate-semiconductor-drain/source metal is  $<1\mu\text{m}$ . In an AMNR (top-down view in second image), the **critical vertical alignment is upper electrode over lower electrode - the tunneling junction**. This dimension is often  $>5\mu\text{m}$ .



# AMNR Performance: Speed. Simplicity. Stability.



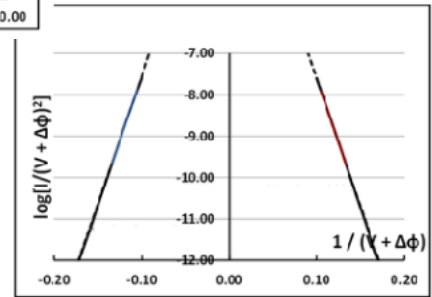
Non linearized IV data format

$$I = A(V + \Delta\phi)^2 e^{\left(\frac{B}{V + \Delta\phi}\right)}$$

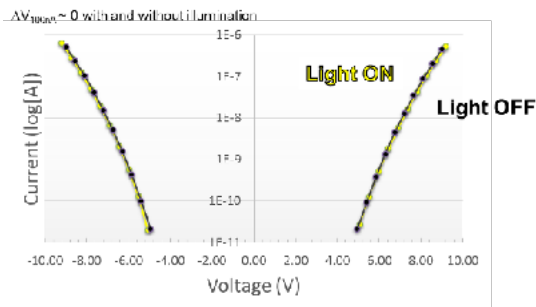
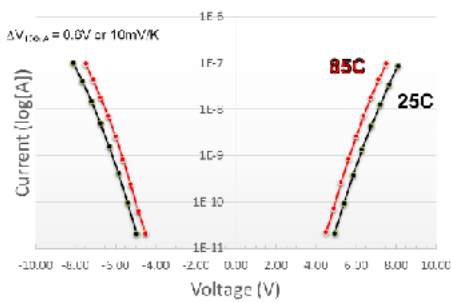
Linearized IV data format

$$\ln \frac{I}{(V + \Delta\phi)^2} = \frac{B}{V + \Delta\phi} + \ln A$$

ln
I
/
(V + Δφ)<sup>2</sup>
=
B
/
V + Δφ
+
ln A



AMNR I-V curve shows 0.9999 correlation to Fowler-Nordheim conduction equation.



The AMNR is a 2-terminal pair of tunneling diodes **sharing an amorphous metal base**. This physical construction guarantees I-V symmetry around 0V/0A - critical for its high-speed, high-reliability performance as a bi-directional switch.

The amorphous metal lower electrode enables the relatively thin insulator required for Fowler-Nordheim tunneling **at voltages typical for LCD and OLED row select lines**. It also ensure **uniform current density distribution across the tunneling junction** - critical to AMNR supporting >50,000 hours of operation in display applications.

The AMNR's current conduction limits are defined by the dimensions of the two tunneling junctions - which are identical in area. **Current conduction scales with tunneling junction area**.

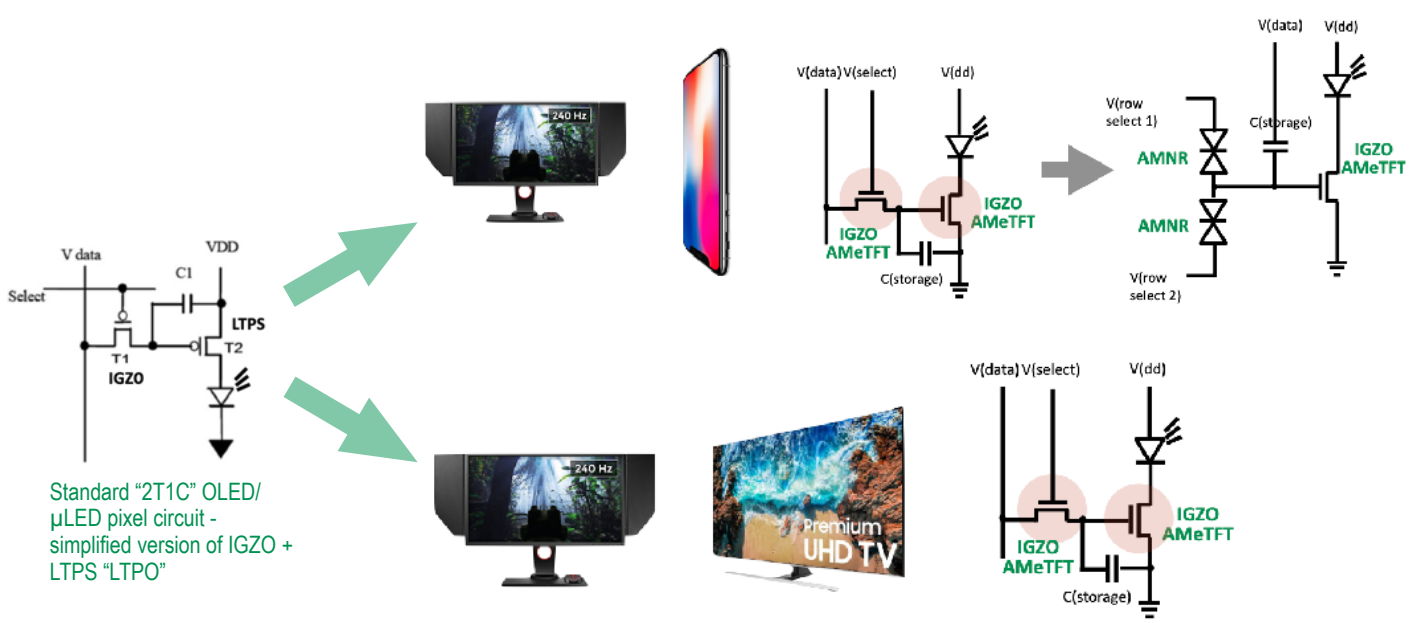
A unique feature of the AMNR's F-N tunneling operation is that switching speed is independent of operating voltage. This redefines the concept of "slew rate" - a change in current responding to a change in voltage over a period of time - **making the AMNR capable of switching at THz rates - never before possible in thin film electronics**.

An AMNR-IPS LCD display built in collaboration with the display industry's largest manufacturer demonstrated the ability to **hold pixel brightness to 8 bits of resolution for > 5 minutes - with the power to the display off**. The AMNR-IPS verifies the theory of minimal leakage current for Fowler-Nordheim tunneling devices.

AMNR 7200sec stress performance across a range of control voltages at 25°C, 80°C and illuminated with 7000 nits of white light. The results show Fowler-Nordheim's relatively low sensitivity to temperature or light.



# Technology Roadmap

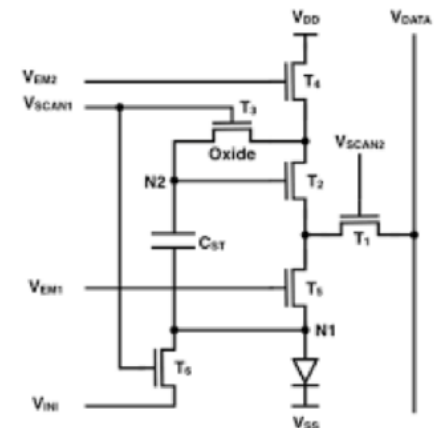


One of the benefits of high-performance thin film devices is their ability to simplify circuit structures without compromising circuit performance.

The high mobility and operating stability of IGZO AMeTFT creates a path to dramatically simplifying the LTPO pixel circuit that is the backplane of choice for premium AMOLED and  $\mu$ LED small-to-medium area displays. **IGZO AMeTFT's leakage current is - like all IGZO TFTs - orders of magnitude lower than LTPS TFT leakage current.**

The relatively high LTPS TFT leakage current requires the added complexity of an in-pixel sample-and-hold circuit to maintain full brightness range over time. **IGZO AMeTFT uniquely replaces LTPS TFTs with LTPS-level mobility that traditional IGZO TFTs do not provide while maintaining IGZO-level stability.** IGZO AMeTFT uniquely enables the traditional 2 TFT/1 capacitor pixel circuit to meet the requirements of premium AMOLED and  $\mu$ LED displays - **including 0.1-240Hz variable image refresh rate.**

Amorphyx's small-to-medium area display roadmap incorporates an even greater level of stability performance as the replacement for IGZO AMeTFT as the row select switch. **The 2 AMNR/1 TFT/1 capacitor "211" pixel circuit enables even wider variable image refresh range.**



Apple's patented Low Temperature Polysilicon Oxide AMOLED/ $\mu$ LED pixel circuit is a 6 TFT/1 capacitor structure. It implements a 1-bit sample-and-hold circuit around the LTPS TFT driving current through the light emitter to compensate LTPS TFT's performance degradation over time. The IGZO ("Oxide") TFT performs the pixel row enable function.



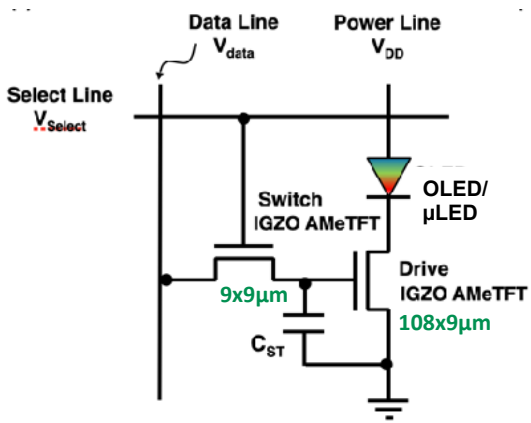
# “2T1C” IGZO AMeTFT: Small-to-Large Area Displays

Improved Image Quality, Cost, Manufacturability compared with LTPO

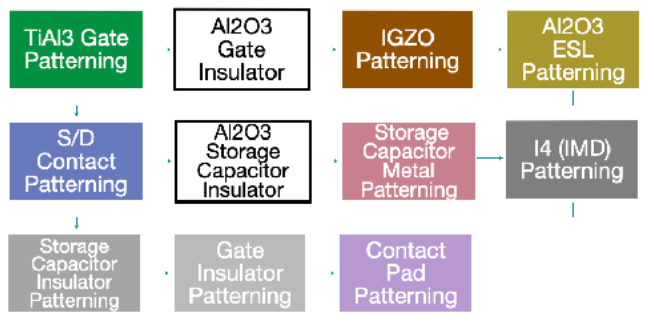
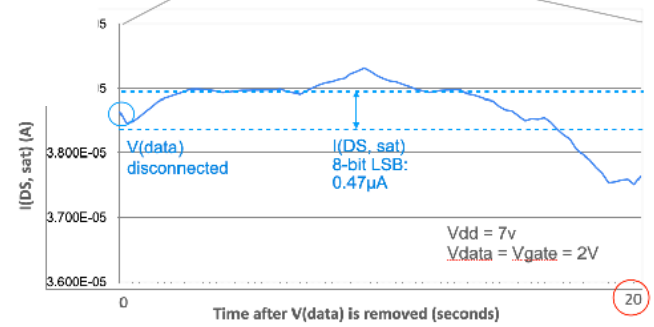
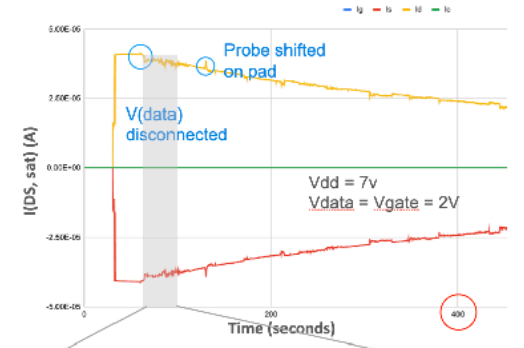
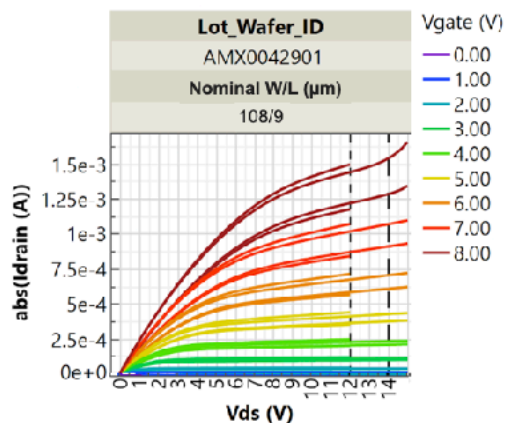
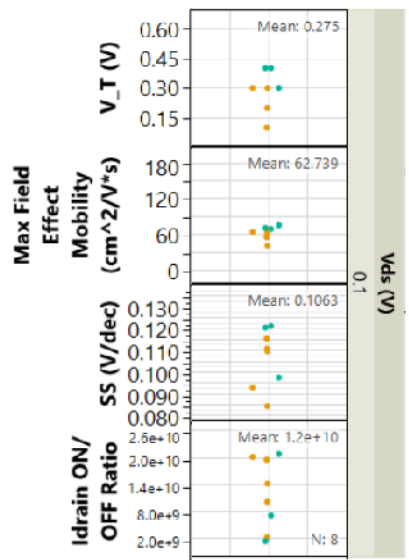
### Key Benefits

- Increases Image Resolution, Refresh Rate
- Improves Manufacturability
- Simplifies Display Manufacturing

- Combines AMNR’s very high switching speed with AMeTFT’s Moore’s Law improvements over standard TFTs for
  - higher refresh rates
  - higher resolutions
  - 50% reduction in mask count relative to LTPO
- Materials system ideal for flexible and rigid displays
- Gate-on-Arry
- Best-in-class leakage performance of AMNR, AMeTFT enables 0.1-120Hz image refresh rates



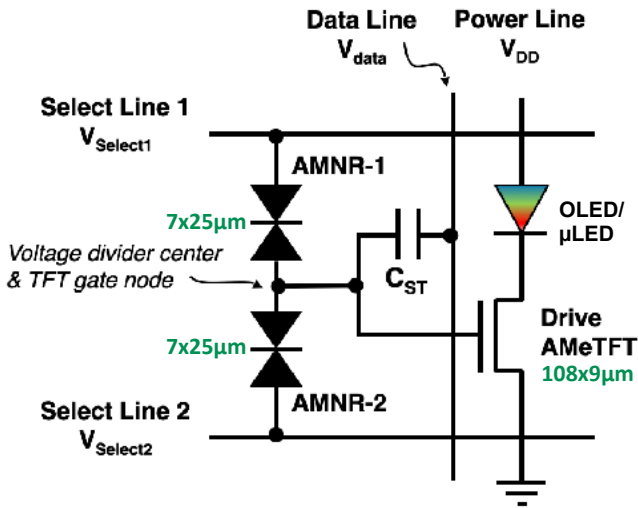
W/L = 108/9µm  
IGZO AMeTFT



$I(ds) @ V(ds)|_{7V}, V(data)|_{2V} = 40\mu A$   
 8 bits  $I(DS)$  resolution - LSB =  $0.47\mu A$   
 After  $V(data)$  probe is disconnected,  $I(ds)$  decays  $0.47\mu A$  after 17 seconds - **0.06Hz image refresh rate**



# “211”: IGZO AMeTFT + AMNR Small-to-Medium Area Displays

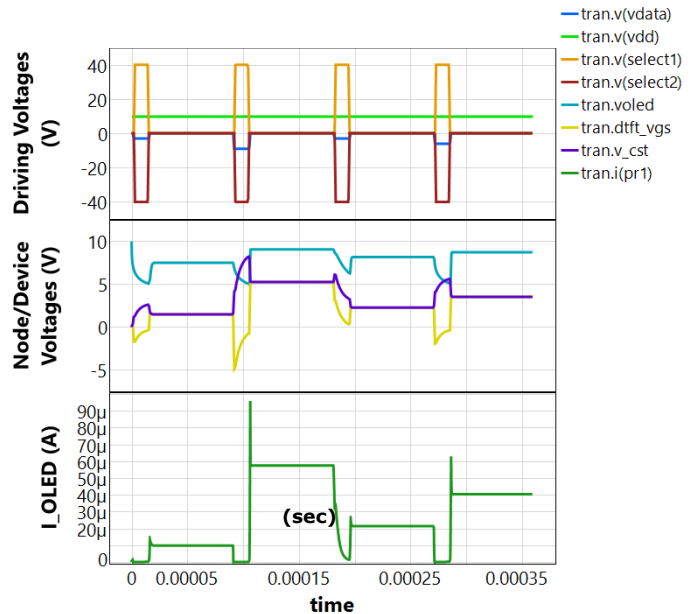
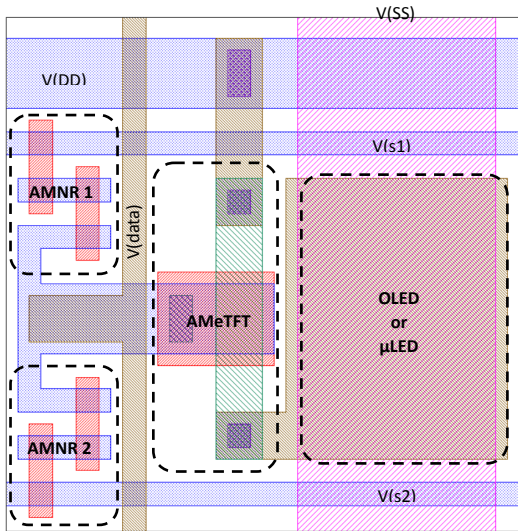


Improved Image Quality, Cost, Manufacturability compared with LTPO

## Key Benefits

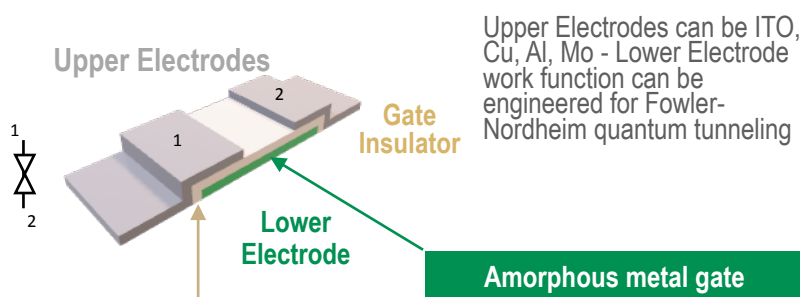
*Increases Image Resolution, Refresh Rate  
Improves Manufacturability  
Simplifies Flexible Display Manufacturing*

- Combines AMNR's very high switching speed with AMeTFT's Moore's Law improvements over standard TFTs for
  - higher refresh rates
  - higher resolutions
  - >50% reduction in mask count relative to LTPO
- Materials system ideal for flexible and rigid displays
- Best-in-class leakage performance of AMNR, AMeTFT enables 0.01-240Hz image refresh rates
- Gate-on-Array





# AMNR-IPS: Gaming Monitors



Upper Electrodes can be ITO, Cu, Al, Mo - Lower Electrode work function can be engineered for Fowler-Nordheim quantum tunneling

- High-k dielectric**
- Al<sub>2</sub>O<sub>3</sub> 100-250Å
  - Room Temperature Sputter
  - <5Å RMS surface roughness

- Amorphous metal gate**
- TiAl<sub>3</sub> 250-500Å
  - Room Temperature Sputter
  - Wet or dry etch

• Reduces leakage current, V<sub>TH</sub> variations related to silicon-based gate insulators

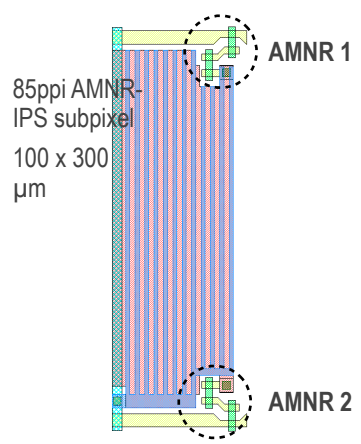
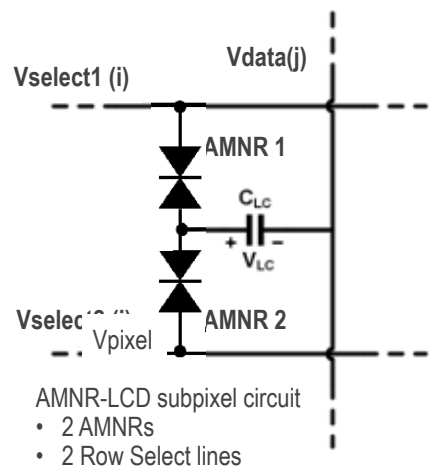
• Enables thinner gate insulator, increasing mobility

## Semiconductor-less Quantum Tunneling Electronics Drives Image Refresh Rates Beyond 240Hz, Simplifies Manufacturing for LCD

### Key Benefits

*Increases Image Resolution, Refresh Rate Improves Manufacturability*

- No semiconductors
  - Reduces performance variations across display backplane, improving image quality uniformity
  - Minimal performance sensitivity to light, temperature - minimal degradation in image quality over display lifetime
- Simple physical structure eliminates vertical alignment photolithography challenges
  - Reduces production line throughput times
- No leakage currents
  - Supports variable image refresh rates
  - Eliminates need for storage capacitor
- Supports VA and IPS structures
  - Patented AMNR-IPS pixel implementation



5" 85ppi AMNR-IPS LCD panel designed and fabricated in collaboration at BOE's G2.5 R&D fab. [Click on image to view YouTube movie of display.](#)



# Intellectual Properties

45 patents granted or in prosecution in



### AMTFT

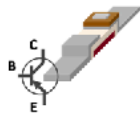
US11183585  
TW201942979  
CN1119119302  
KR20200130466  
JP2021520060

### Semiconductor Smoothness

US2021053815  
TW2021110137212  
PCT/US2021053815

### Amorphous Metal Top Emission OLED

US202263311783P



### AMHET

US11069799  
US10672898  
CN109564892  
KR20190018008  
TWI678738  
JP2019525461



### AMIM

US8436337  
US8822978

### AMNR

US9099230  
JP6212125  
CN10526461  
TWI532063  
KR20150084879

### AMNR-X

US10438841  
US10777448  
US10971392  
US10937687  
TWI669782  
JP6692439  
CN108352358  
KR102147141



### "211" AMNR+AMTFT

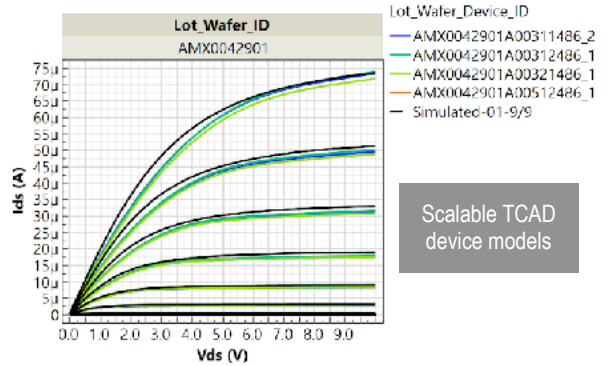
US2021037065  
TW2021110121473  
WO2021252934

### AMNR-based Circuits

US201862776931  
US20220028345  
TW202029172  
CN113272884  
KR20210090272  
WO2020118268

### AMNR-IPS

US10234734  
TWI639875  
JP2018524642  
KR20180025988  
CN107924094



Scalable TCAD device models

Granted  
In Prosecution

Multi-Variant Analysis Database

	Controllab	Increment	Min	Max	Chosen value	Increment	Starting	Impact on mobility	Impact on Vth	Impact on PBTS	Impact on NBTS	Impact on mobility	Impact on Vth	Impact on PBTS	Impact on NBTS	
S1 thickness	Yes	5nm increments	20	50	46.26	50.00	40.00									
S1 O2	Yes	.25% increments	1	10	6.54	6.75	3.00	0.45			0.04	22	0	0	2	
I1 O2	Yes	.25% increments	5	15							0.53				4	
I1 thickness	Yes	5nm increments	50	100							-0.59				-6	
ESL O2	Yes	.25% increments	20	40							0.01				1	
ESL thickness	Yes	2nm increments	10	20							0.55				8	
S1 pressure	Yes	0.2 mTorr	3.25	5							-0.35				-2	
Post processing anneal temp	Yes	1 degree	120	150	177.89	178.00	174.00	0.11	-0.13	1.78		19	-23	317	0	
Process processing anneal time	Yes	1 minute	60	120	119.76	120.00	120.00	0.80		0.02		96	0	0	0	
Stress voltage			-30	30												
Coefficient																
												Achieved	-40	23	-385	-7
													56.9	0.1	-0.7	-1.0
												Target	0	0	0	0
												Difference	-0.1	-0.7	-1.0	
												Amount deviation outside 1	0.1	0.7	1.0	
												Outside 1	0.0	0.0	0.0	
												Optimal	56.9			





# Collaboration

	Research Collaboration	Product Collaboration	Product Optimization	Pilot Production	Production
<b>Objective</b>	Fabricate Amorphyx technology-based display backplane at customer R&D fab	Fabricate display proof-of-concept to customer specifications using Amorphyx technology-based backplane		Prepare product using Amorphyx technology-based backplane for mass production	Mass production of product using Amorphyx technology-based backplane
<b>Commercial Terms</b>	<ul style="list-style-type: none"> <li>12-month Research Collaboration License</li> <li>Payment at Agreement</li> <li>Fee per spec-compliant film</li> <li>Fee for spec-compliant backplane array</li> </ul>	<ul style="list-style-type: none"> <li>Product-specific Product Development License</li> <li>per-quarter fee</li> </ul>		<ul style="list-style-type: none"> <li>Product-specific, fabrication facility-specific Production License</li> <li>per-quarter fee</li> </ul>	<ul style="list-style-type: none"> <li>Product-specific, fabrication facility-specific Production License</li> <li>per-square-meter of manufactured display royalty</li> <li>Royalty buyout option after meeting minimum volumes</li> </ul>

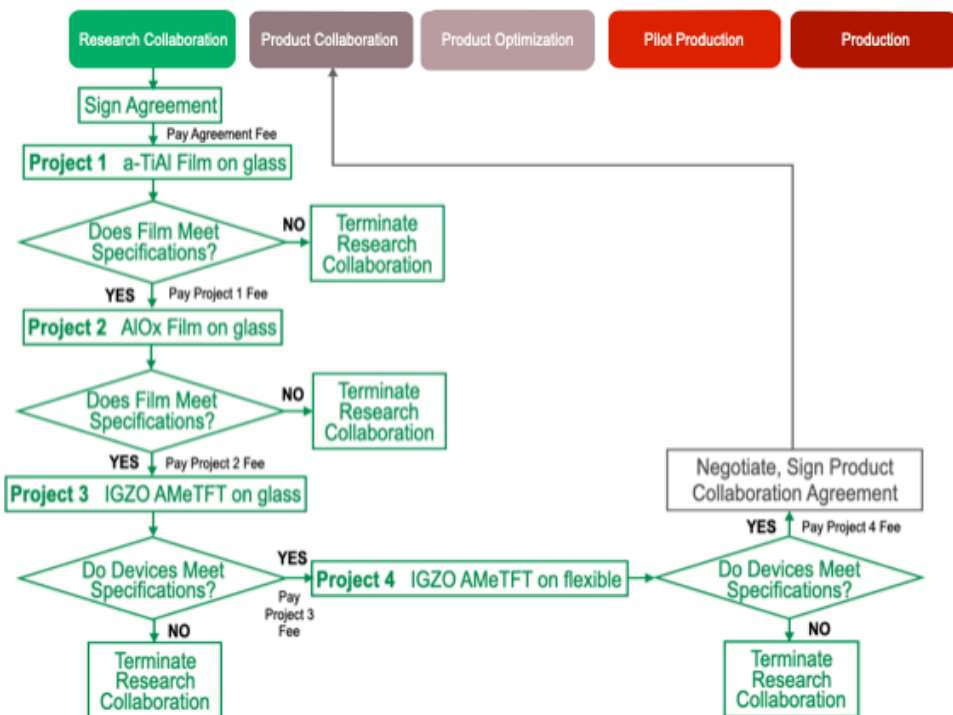
The foundation of Amorphyx's thin film device technologies is **the ability to efficiently and effectively transfer them to the customer's fabrication line.**

We set this foundation through **tools designed to give the customer full access** to the results of our research and development programs:

- online access to the Amorphyx database relating thin film parameters to device electrical performance;
- online access to Amorphyx's proprietary theoretical models for understanding the relationships between thin film parameters and device electrical performance; and
- SPICE-compatible device models for circuit design.

The first phase of a customer relationship - Research Collaboration - establishes the Amorphyx technology on the customer's fabrication line. This empowers the customer's Technology team to immediately gain full understanding of Amorphyx technologies for supporting the customer's Operations team.

**Research Collaboration is designed to minimize the risk of the customer's financial and time investment in Amorphyx technology.** A timely and successful Research Collaboration empower the customer's Technology team to best support Operations.



Contact CEO John Brewer [jbrewer@amorphyx.com](mailto:jbrewer@amorphyx.com) for more information on collaboration opportunities